ABSTRACT

0028 A single transistor planar RAM memory cell with improved charge retention and a method for forming the same, the method including providing forming a pass transistor structure adjacent a storage capacitor structure separated by a predetermined distance; carrying out a first ion implantation process to form first and second doped regions adjacent either side of the pass transistor structure, the first doped region defined by the predetermined distance; depositing a spacer dielectric layer; etching back the spacer dielectric layer to leave an unetched spacer dielectric layer portion overlying the first doped region while forming a sidewall spacer of a predetermined width overlying a first portion of the second doped region; and, carrying out a second ion implantation process to form a relatively higher dopant concentration in a second portion of the second doped region.